ANALYSIS AND DESIGN OF LOW POWER FLIP-FLOP BASED ON SLEEPY STACK APPROACH

P.Sindhu1, K.Banupriya2

1 Professor, Electronics and communication Engineering, Nehru Institute of Technology, Coimbatore, Tamil Nadu, India.

2 Student, VLSI Design, Nehru Institute of Technology, Coimbatore, Tamil Nadu, India.

Abstract **-** Low power is an important principal theme in today's electronics industry. So this Low Power Pulse Triggered Flip Flop reviews various methodologies for designing low power circuits and systems. It describes the many issues facing designers at architectural, logic, circuit and device levels and presents some of the techniques that have been proposed to overcome these difficulties. This paper concludes with the future challenges that must been met to design low power, high performance systems. In the existing method conventional explicit type pulse triggered FF (P-FF) design with clock gating technique are used. This method has been some disadvantages like high leakage power and delay . To obtain balanced performance among power, delay, and area, design space exploration is also a widely used. In a synchronous circuit dynamic power is consumed by a major source of clock power. Clock-gating technique was used to reduce clock power. Thus significant amount of power consumption is reduced by using clock gating technique. The proposed sleepy stack approach with edge trigger flip-flop design is used to solve the leakage power problem and reduce delay and current with different voltages. Because sleepy stack mode will employ to save the leakage power.

Keyword **-** Flip-Flop, clock gating, edge trigger design, sleepy stack approach.

1. INTRODUCTION

Flip-flops (FFs) [1] are the basic storage elements that are used extensively in all kinds of digital designs. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is higher than as z50% of the total system power. FFs thus contribute a significant portion of the chip area and power Consumption to the overall system design. Pulse-triggered FF (P-FF),[2] because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. In a statistical design framework is developed to take these factors into account. To obtain balanced performance among power, delay, and area, design space exploration is also a widely used technique. In this brief,[3] we present a novel low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data "1"and "0," the design manages to shorten the longer delay by feeding the Input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass transistor for extra signal driving. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power-delay-product (PDP) performances. Flip-flops[4] are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data. At each rising or falling edge of a clock signal, the data stored in a set of Flip-Flops is readily available so that it can be applied as inputs to other combinational or sequential circuitry. Such flip-flops that store data on both the leading edge and the trailing edge of a clock pulse are referred to as double-edge triggered Flip-Flops otherwise it is called as single edge triggered Flip-Flops. A triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. Leakage power[5] consumption of current CMOS technology is already a great challenge. ITRS projects that leakage power consumption may come to dominate total chip power consumption as the technology feature size shrinks. We propose a novel leakage reduction technique, named "sleepy stack," which can be applied to general logic design. Our sleepy stack approach retains exact logic state making it better than traditional sleep and zigzag techniques while saving leakage power consumption. Unlike the stack approach (which saves state), the sleepy stack approach can work well with dual-Vth technologies, reducing leakage by several orders of magnitude over the stack approach in single-Vth technology. Unfortunately, the sleepy stack approach does have a area penalty as compared to stack technology; nonetheless, the sleepy stack approach occupies a where state-saving and extra low leakage is desired at a (potentially small) cost in terms of increased delay and area.

2. RELATED WORKS

V. Stojanovic and V.Oklobdzija[1] proposed Master–slave latches and flip flops illustrate the advantages of our approach and the suitability of different design styles for high performance and low power applications. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master-slave configuration. A goal of making the comparisons fair and realistic. Simulation of the latches and flip-flops. The suitability of different design styles for high-performance and low-power applications. This provides us with a good illustration of the total power dissipated in the latch and its surroundings. It is that there is very little performance penalty for embedded logic functions. The major disadvantages are bigger clock load and larger effective precharge capacitance.

M.-W. Phyu, W.-L. Goh, and K.-S. Yeo[2] motivated , a new family of edge-triggered flip-flops has been developed. The flip-flops belong to a class of semi dynamic and dynamic circuits that can interface to both static and dynamic circuits. The main features of the basic design are short latency, small clock load, small area, and a single-phase clock scheme. Furthermore, the flip-flop family has the capability of easily incorporating logic functions with a small delay penalty. since each flip-flop can be viewed as a special logic gate that serves as a synchronization element as well. This feature greatly reduce the pipeline overhead, a new family of edge-triggered flip-flops has been developed. The flip-flops belong to a class of semi-dynamic and dynamic circuits that can interface to both static and dynamic logic. The term semi-dynamic is used here to denote circuits that internally have a pre-charge and evaluation phase, similar to dynamic gates. Higher clock rates and higher performances are obtained.

H. Mahmoodi, V. Tirumalashetty[3] approach is The ultra low power can reduce the clock system power of a VLSI down to one-third compared to the conventional flip-flop. This power improvement is achieved through the reduced clock swing down to 1 V. The area and the delay of the clock gating can also be reduced by a factor of about 20% compared to the conventional flip flop. The RCSFF can also reduce the RC delay of a long RC interconnect to one-half**.** Reduced clock-swing flip-flop is proposed to lower the voltage swing of the clock system. This is because the power consumption of the clock system is proportional either to the clock swing or to the square of the clock swing, depending on the circuit configuration. The clock gating is composed of a true single-phase master-latch and a cross coupled NAND slave-latch. The master-latch is a current latch-type sense-amplifier. The salient feature of the clock gating is that it can accept a reduced voltage swing due to the single-phase nature of the flip-flop. It can reduce the clock system power of a VLSI down to one-third compared to the conventional Flip-flop.

Anurag, Gurmohan Singh, V.Sulochana[4] aims to enumerates new architecture of low power dual-edge triggered Flip-Flop (DETFF) designed at 180nm CMOS technology. In DETFF same data throughput can be achieved with half of the clock frequency as compared to single edge triggered Flip-Flop (SETFF). In this paper conventional and proposed DETFF are presented and compared at same simulation conditions. The proposed DETFF design is suitable for low power and small area applications. Power dissipation is improved. High clock frequency and Decrease the speed of the design.

G.Venkadeshkumar, K.Pandiara[5] project tries to model the low power pulse triggered flip-flop (P-FF) design is done by the pulse generation control logic, an AND function, is removed from the critical path to facilitate a faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. A conditional pulse enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse generation circuit can be reduced for power saving. Various post layout simulation results based on UMC CMOS 90-nm technology reveal that the enhanced pulse triggered FF design features the best power-delay-product performance in seven FF designs under comparison. Its maximum power saving against rival designs is up to 38.4%. Transistor sizes in delay inverter and pulse generation circuit can be reduced for power saving. Compared with the conventional Transmission gate based flip-flop design. The average leakage power Consumption is also reduced by a factor of 3.52. High performance of primary interest within a certain power budget. Full fledge Reliability.

3. PREVIOUS WORK

Conventional explicit type pulse trigger flip-flop with clock gating technique is a existing method. In this method, the signal feed through scheme and boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened. Although this seems to burden the input source with direct charging/discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case because MNx conducts only for a very short period. When a “1” to “0” data transition occurs, transistor MNx is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of “0” to “1” data transition, the input source bears the sole discharging responsibility. Since MNx is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted. this method solve the long discharge path but it will produce more leakage power and delay will be increase.

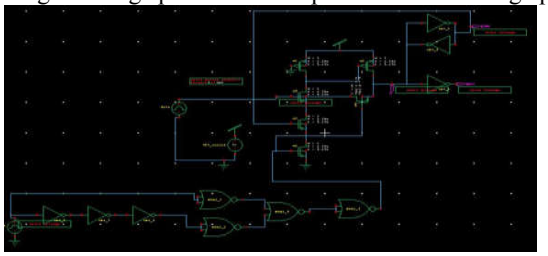

Fig.1 CEPFF with Clock Gating

4. PROPOSED METHODOLOGY

The proposed methodology in this paper is sleepy stack approach. The proposed work can be divided into techniques that either (i) preserve state or (ii) destroy state. In this section, our new low-leakage-power design, named "sleepy stack," is described. The idea of the sleepy stack technique is to combine the sleep transistor approach during active mode with the stack approach during sleep mode. The structure of the sleepy stack approach is shown in Fig.2 the sleepy stack technique divides existing transistors into two transistors each typically with the same width *W*1 half the size of the original single transistor's width *W*2 (i.e., *W*1 = *W*2/2). Then sleep transistors are added in parallel to one of the transistors in each set of two stacked transistors.

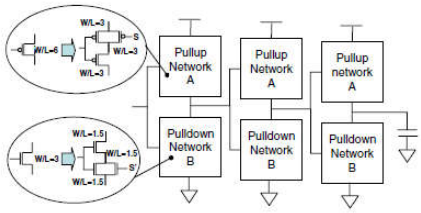

Fig.2 Sleepy Stack

See Fig.3 for an example. The divided transistors reduce leakage power using the stack effect while retaining state. The added sleep transistors operate similar to the sleep transistors used in the sleep technique in which sleep transistors are turned on during active mode and turned off during sleep mode. Fig.3 depicts the sleepy stack operation using an inverter. During active mode, *S*=0 and *S*_=1 are asserted, and thus all sleep transistors are turned on. Due to the added sleep transistor, the resistance through the activated path decreases, and the propagation delay decreases (compared to not adding sleep transistors while leaving the rest of the circuitry the same, i.e., with stacked transistors). During the sleep mode, *S*=1 and *S*_=0 are asserted, and so both of the sleep transistors are turned off. The stacked transistors in the sleepy stack approach suppress leakage current.

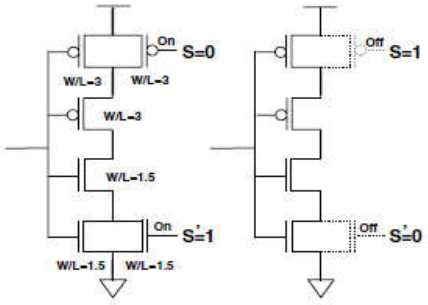

Fig.3 Sleepy Stack Active Mode (Left) And Sleep Mode (Right)

5. EXPERIMENTAL METHODOLOGY

The sleepy stack approach is applicable to general logic design, like edge trigger design. The edge trigger flip-flop with sleepy stack diagram shown in fig.4. the simulation diagram explain about leakage power reduction and power saving using the inverter. pull up and pull down network connected to the sleep and stack method. When the clock pulse is '0' the entire pMOS transistor are ON and nMOS transistor are OFF. We change the clock pulse '1'pMOS transistor are OFF and nMOS transistor are ON. The output Q will change (QB). Then the buffer will used to save the power and reduce the leakage power. In this sleepy stack method used to reduce the leakage power and delay.

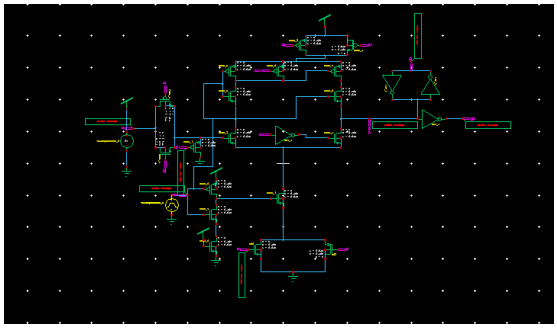

Fig.4 Edge Trigger Design With Sleepy Stack Technique

6. EXPERIMENTAL RESULTS

We measure worst case propagation delay and power using sleepy stack method. Dynamic power is measured with a random input vector changing every clock cycle. Sleepy stack approaches are also implemented using dual-*Vth* technology. The main advantage of the sleepy stack approach is that dual-*Vth* technology can be effectively applied to the sleepy stack, resulting in three orders of magnitude reduction in leakage power is reduced when compared to the pulse trigger FF with clock gating tech. Therefore, our sleepy stack approach with dual-*Vth* can be used where state-preservation and ultra-low leakage power consumption are needed and are judged to be worth the area overhead. One observation we notice from the results is that none of the approaches shows the best result in all criteria. Designers need to choose an appropriate technique for a given technology and a particular chip. Our sleepy stack approach provides a new low-power VLSI design technique to achieve significant leakage power reduction in deep sub-micron while achieving either (i) saving of state (unlike sleep and zigzag) or (ii) lower delay than a straight forward stack approach.

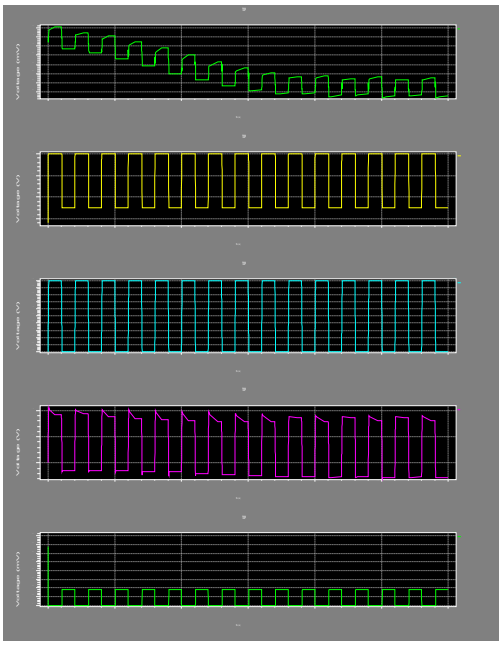

Fig.5 Output of sleepy stack

TABLE 1
VOLTAGE ANALYSIS OF VARIOUS FF

CETPFF			
Voltage sources(v)	5v	4v	3v
Current(ma)	0.653	0.523	0.395
Power(mw)	0.741	0.473	0.264
ETFF			
Voltage sources(v)	5v	4v	3v
Current(ma)	0.148	0.118	0.088
Power(mw)	0.326	0.209	0.185

7. CONCLUSION

In nanometer scale CMOS technology, leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques base upon technology and design criteria. Our novel sleepy stack, which combines the sleep and the stack approaches, is proposed as a new choice for logic designers. Furthermore, the sleepy stack is applicable to single and multiple threshold voltages.

In conclusion, the sleepy stacks combine some of the advantages of sleep transistors – most notably the effective use of dual-*Vth* technology–with some of the advantages of the stack approach is the ability to save state. As such, the sleepy stack approach represents a new weapon in the VLSI designer's repertoire.

ACKNOWLEDGEMENT

I acknowledge Nehru Institute of technology and my guide for the support and permission to utilize laboratory resources.

REFERENCES

1.V. Stojanovic and V. Oklobdzija,"Comparative analysis of masterslave latches and flip-flops for high-performance and low-power systems," IEEE J. Solid-state Circuits, Vol. 34, No. 4, Pp. 536–548,apr. 1999.
2.M.-W. Phyu, W.-L. Goh, and K.-S. Yeo, "A low-power static dual edgetriggered flip-flop using an output-controlled discharge configuration," in Proc. IEEE Int. Symp. Circuits Syst., May 2005, pp.
3.H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra lowpower clocking scheme using energy recovery and clock gating," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 1, pp. 33–44,Jan. 2009.
4.N. S. Kim et al., "Leakage Current: Moore's Law Meets Static Power," IEEE Computer, Vol. 36, Issue 12, pp. 68-75, December 2003.
5.Anurag, Gurmohan Singh. Sulochana "Low Power Dual Edge-triggered Static D Flip-flop" International Journal Of VLSI design &Communication Systems(VLSICS) Vol.4,No.3,June 2013.
6. International Technology Roadmap for Semiconductors by Semiconductor Industry Association, http://public.itrs.net, 2002.
7. L. T. Clark et al., "An Embedded 32-b Microprocessor Core for Low-Power and High-Performance Applications," IEEE Journal of Solid-State Circuits, Vol. 36, No. 11, pp. 1599-1608, November 2001.
8. M. Powell, S.-H. Yang, B. Falsafi, K. Roy and T. N. Vijaykumar, "Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep-submicron Cache Memories," International Symposium on Low Power Electronics and Design, pp. 90-95, July 2000.
9. S. Mutoh et al., "1-V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solis-State Circuits, Vol. 30, No. 8, pp. 847-854, August 1995.
10. Z. Chen, M, Johnson, L. Wei and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks," International Symposium on Low Power Electronics and Design, pp. 239-244, 1998.
11. S. Narendra, S. Borkar, V. De, D. Antoniadis and A. Chandrakasan, "Scaling of Stack Effect and its Application for Leakage Reduction," International Symposium on Low Power Electronics and Design, pp. 195-200, August 2001.
12. M. Johnson, D. Somasekhar, L-Y. Chiou and K. Roy, "Leakage Control with Efficient Use of Transistor Stacks in Single Threshold CMOS," IEEE Transactions on VLSI Systems, Vol. 10, No. 1, pp. 1-5, February 2002.
13. K.-S. Min, H. Kawaguchi and T. Sakurai, "Zigzag Super Cut-off CMOS (ZSCCMOS) Block Activation with Self-Adaptive Voltage Level Controller: An Alternative to Clock-gating Scheme in Leakage Dominant Era," IEEE International Solid-State Circuits Conference, Vol. 1, pp. 400-401, February 2003.
14. K. Flautner, N. S. Kim, S. Martin, D. Blaauw and T. Mudge, "Drowsy Caches: Simple Techniques for Reducing Leakage Power," International Symposium on Computer Architecture, pp. 148-157, May 2002.
15. Y. Cao, T. Sato, D. Sylvester,M.Orshansky, and C. Hu, "New paradigm of predictive MOSFET and interconnect modeling for early circuit design," Proc. of IEEE CICC, pp. 201-204, June 2000.
16. P.Pfeiffenberger, J. Park and V. Mooney, "Some Layouts Using the Sleepy Stack Approach," Technical Report GIT-CC-04-05,